(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 322 116**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88311138.7

(51) Int. Cl.4: G06F 15/16

(22) Date of filing: 24.11.88

(30) Priority: 22.12.87 US 136701

(43) Date of publication of application:
28.06.89 Bulletin 89/26

(84) Designated Contracting States:
AT BE CH DE ES FR GB GR IT LI LU NL SE

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(54) Interconnect system for multiprocessor structure.

(57) An improved digital data processing apparatus has a plurality of processing cells, at least one of which includes a central processing unit (2), an associated memory element (2), and a cell interconnect element (12). The processing cells are coupled in a ring configuration on a bus which includes a shift register element having a set of digital storage and transfer stages connected in series. These stages sequentially store and transfer digital signals applied to the bus. The cell interconnect element is arranged for sending digital signals on the bus by way of the shift register.

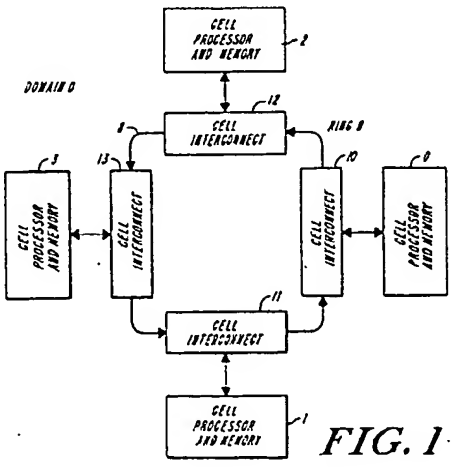

FIG. 1

EP 0 322 116 A2

PUB-NO: EP000322116A2

DOCUMENT-IDENTIFIER: EP 322116 A2

TITLE: Interconnect system for multiprocessor structure.

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Abstract Text - FPAR (1):

CHG DATE=19990617 STATUS=O> An improved digital data processing apparatus has a plurality of processing cells, at least one of which includes a central processing unit (2), an associated memory element (2), and a cell interconnect element (12). The processing cells are coupled in a **ring** configuration on a bus which includes a **shift register** element having a set of digital storage and transfer stages connected in **series**. These stages sequentially store and transfer digital signals applied to the bus. The cell interconnect element is arranged for sending digital signals on the bus by way of the shift register.

Application Date - APD (1):

19881124